AN-6902
Applying SG6902 to Control a CCM PFC and Flyback/PWM Power Supply

Summary

This application note shows a step-by-step design to a 120W/24V power adapter. The equations also can be applied to different output voltages and wattages.

Features

- Interleaved PFC/PWM Switching
- Green-Mode PFC/PWM Switching
- No PFC Switching at Light Loads for Power Saving
- Innovative Switching Charge Multiplier-divider
- Low Startup and Operating Current
- Innovative Switching Charge Multiplier-divider
- Multi-vector Control for Improved PFC Output Transient Response
- Average-Current-Mode Control for PFC
- Programmable Two-Level PFC Output Voltage to Achieve the Best Efficiency
- PFC Over-voltage and Under-voltage Protections
- PFC and PWM Feedback Open-loop Protection
- Cycle-by-cycle Current Limiting for PFC/PWM
- Slope Compensation for PWM
- Maximum Power Limit for PWM
- Brownout Protection
- Over Temperature Protection
- Power-on Sequence Control and Soft-start
- 20-Pin SOP and SSOP Packages

Description

SG6902 is designed for power supplies that consist of boost PFC and flyback PWM. It requires few external components to achieve green-mode operation and versatile protections and compensations.

The proprietary interleave switching synchronizes the PFC and PWM stages and reduces switching noise. At light loads, PFC stage is turned off to save power and the PWM switching frequency is decreased in response to the load.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop. The overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, SG6902 shuts off the switching to protect the power supply and its load.

For the flyback PWM stage, the synchronized slope compensation ensures the stability of the current loop. “Hiccup” operation limits a maximum output power during the overload situations.

The difference between members of this family are shown in the table below.

Parameter	SG6902	SG6901A
Start Threshold Voltage	16V	12V
Minimum Operating Voltage	10V	10V
The Interval of OPFC Lags Behind OPWM at Startup	11.5ms	11.5ms
PFC On/Off	O	X
OTP	O	O
Soft-Start	O	O

Pin Configuration

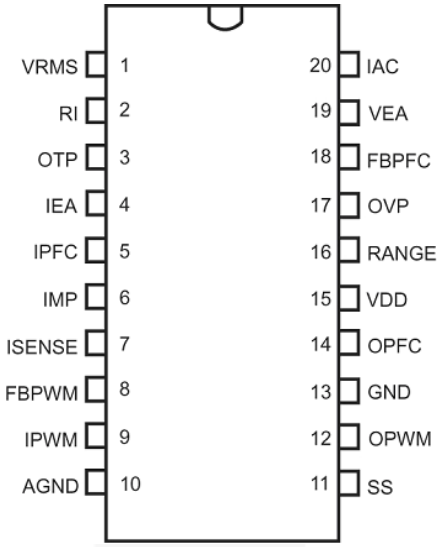

Figure 1. Pin Configuration

Typical Application

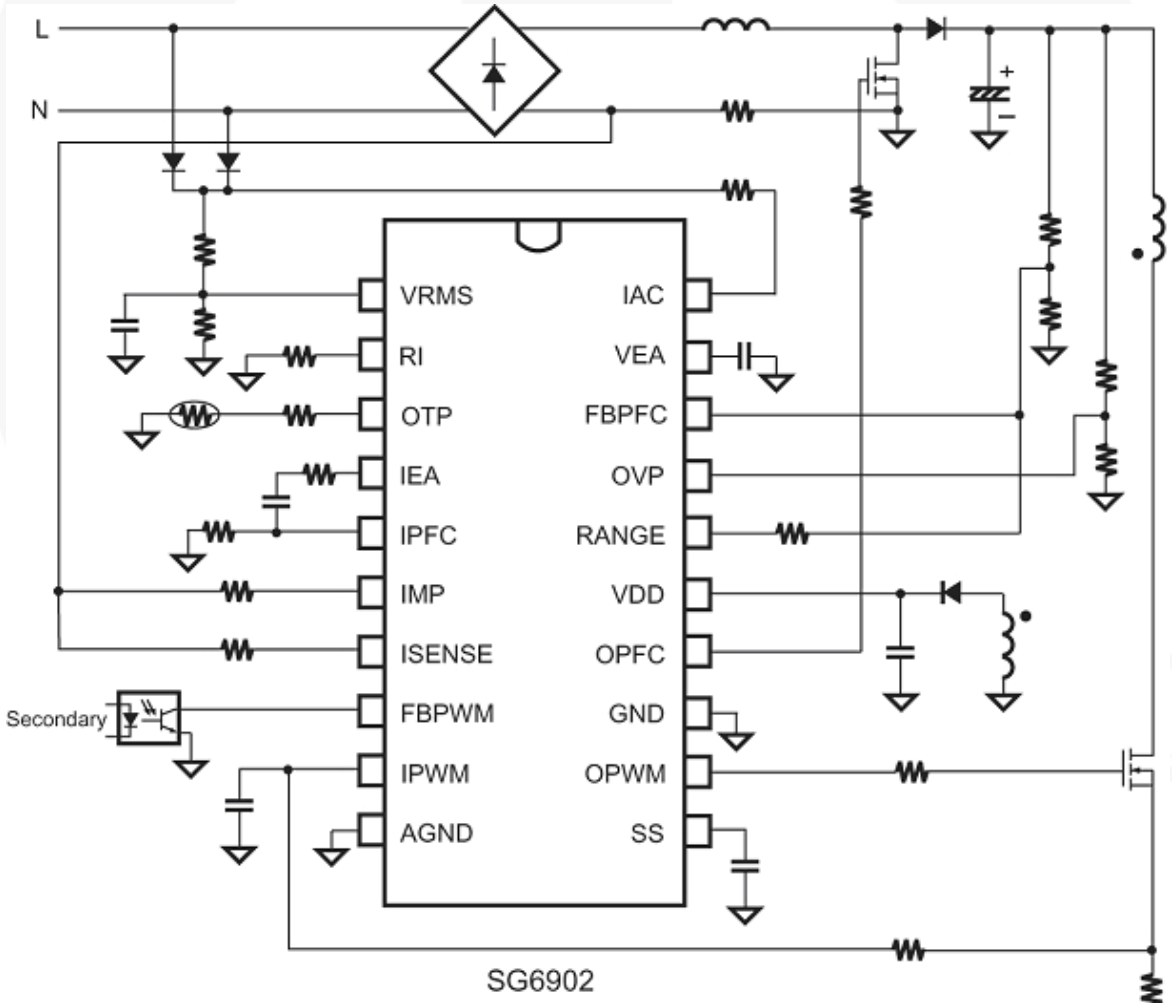

Figure 2. Typical Application

Block Diagram

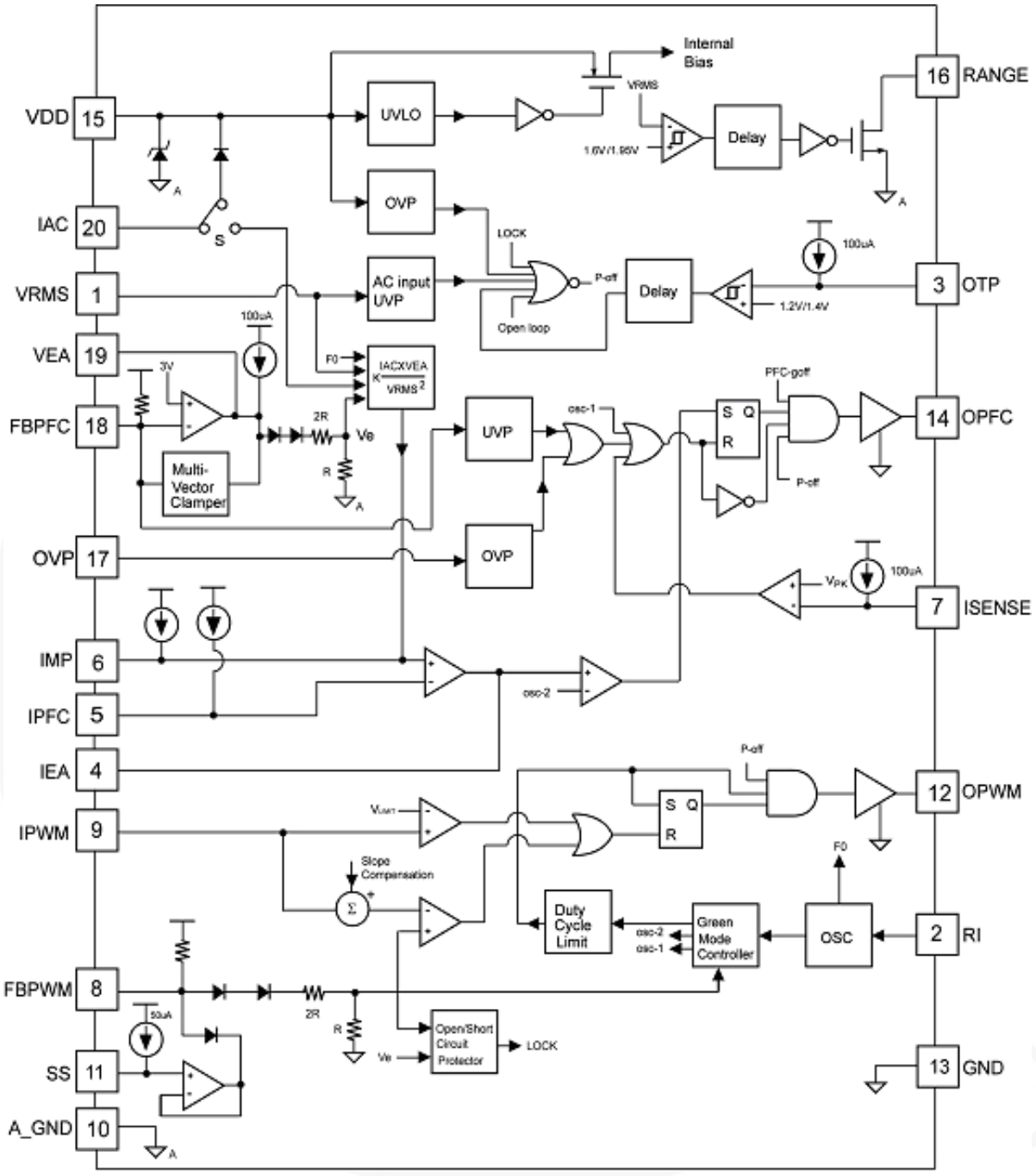

Figure 3. Block Diagram

PFC Section

Power-On Sequence

SG6902 is active when the line voltage is higher than the brownout threshold. The PWM stage is switching first, then, following an 11.5ms delay time after FBPWM voltage is higher than a PFC turn-on threshold voltage, the PFC stage is enabled.

PFC Inductor

The switching frequency f_S, output power P_{OUT}, efficiency *n*, maximum ripple current ΔI, and minimum input voltage $V_{IN.min}$ should be defined before determining the inductance of PFC inductor. The following equations are utilized to determine the inductance of the PFC inductor. Normally the maximum ripple current is 20% ~ 30% of maximum input current.

$$\Delta I = \frac{\sqrt{2}(P_{OUT}/\eta \times 0.3)}{V_{IN(MIN)}} \quad (1)$$

$$D = 1 - \frac{V_{IN.min} \times \sqrt{2}}{V_O} \quad (2)$$

$$V = L\frac{di}{dt} \quad (3)$$

$$L = \frac{V_{IN.min} \times \sqrt{2} \times D_{max}/fs}{\Delta I} \quad (4)$$

For a 120W adapter power, $\eta = 0.85$, $V_{IN(MIN)} = 90V_{AC}$, $f_S = 65KHz$, $V_O = 250V$, $\Delta I = 0.66A$, D = 0.49, L = 0.4mH.

PFC Capacitor

An advantage of using interleaving switching of PFC and PWM stage is to reduce the switching noise. The ESR requirement of boost capacitor is relaxed. The boost capacitor value is chosen to remain a hold-up time of output voltage in the event line voltage is removed.

$$C_O = \frac{2 \times (P_{OUT}/\eta_{PWM}) \times t_{hold\text{-}up}}{(V_{O(normal)} - V_{ripple})^2 - V_{O.min}{}^2} \quad (5)$$

where $V_{O.min}$ is the minimum output voltage in accordance with the requirement of the specification.

For a 120W power supply, the capacitor is determined as:

$$C_O > \frac{2 \times (120W/0.85) \times 15ms}{(250-20)^2 - 60^2} = 86\mu F \quad (6)$$

Because the capacitor includes ±20% variation, the capacitor 100μF is chosen.

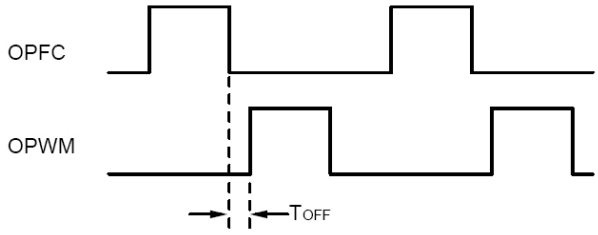

Figure 4. Interleaving Switching

Boost Rectifier and Switch

The fast reverse-recovery time of the boost diode is required to reduce the power losses and the EMI. A 500V voltage rating is chosen to withstand 400V boosts potential. The average current and peak currents flow through the boost diode and the switch, respectively, and are given by:

$$I_{AVG} = \frac{2 \times \sqrt{2} \times P_{OUT}/\eta}{\pi \times V_{RMS(Brownout)}}$$
$$I_{AVG} = \frac{2 \times \sqrt{2} \times 120/0.8}{\pi \times 75} = 1.8A$$
$$I_{PEAK} = \sqrt{2} \times \frac{P_{OUT}/\eta}{V_{RMS(Brownout)}}$$
$$I_{PEAK} = \sqrt{2} \times \frac{120/0.8}{75} = 2.82A \quad (7)$$

Oscillation and Green Mode

The resistor R_I connected from the RI to GND pin programs the switching frequency of SG6902.

$$f_s = \frac{1560}{R_I(K\Omega)}(KHz) \quad (8)$$

For example, a 24kΩ resistor R_I results in a 65kHz switching frequency. The recommended range for the switching frequency is 33kHz ~ 100kHz.

SG6902 provides an off-time modulation to reduce the switching frequency in light-load and no-load conditions. The feedback voltage of FBPWM pin is taken as reference. When the feedback voltage is lower than about 2.1V, the switching frequency decreases accordingly. Most of losses in a switching-mode power supply are proportional to the switching frequency; therefore, the off-time modulation reduces the power consumption of the power supply in light-load and no-load conditions. For a typical case of R_I = 24KΩ, the switching frequency is 65kHz at nominal load and decreases to 20kHz at light load. The switching signal is disabled if the switching frequency falls below 20KHz, which avoids acoustic noise.

For stability reasons, a capacitor connecting the RI pin to GND is not suggested.

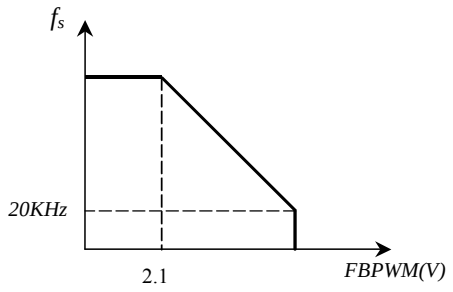

Figure 5. Switching Frequency vs. FB Voltage

To save power, the PFC stage is enabled only when the feedback voltage of the FBPWM pin is higher than a threshold voltage V_{TH}. The threshold voltage V_{TH} is 2.1V to 2.45V at low line voltage input, 1.95V at high line voltage. The threshold voltage V_{TH} determines an output power threshold to turn on/off the PFC stage for the power saving. The output power P_{OUT} can be expressed as:

$$P_{OUT} = \frac{\eta \times (V_{IN} \times t_{ON})^2}{2 \times L_P \times t} \quad (9)$$

$$V_{FB} = 1.2V + 3 \times \left\{ \frac{V_{IN(PEAK)}}{L_P} \times R_S \times t_{ON} + \frac{V_{SL}}{t} \times t_{ON} \right\} \quad (10)$$

where V_{SL} is a synchronized 0.5V ramp.

Equation 10 shows that, through the feedback loop, the on-time t_{ON} changes in response to the change of the switching period t and/or the inductance L_P (the primary inductance of the transformer) for providing a same output power. Because the feedback voltage V_{FB} controls the on-time t_{ON}, a lower V_{FB} causes a narrow on-time t_{ON}. Changing the switching frequency (the switching period t) and the inductance L_P, affects the output power threshold to on/off the PFC stage.

I_{AC} Signal

Figure 6 shows that the I_{AC} pin is connected to the input voltage via a resistor. A current I_{AC} is used for PFC multiplier.

$$I_{AC(PEAK)} \approx \frac{V_{IN(PEAK)}}{R_{AC}} \quad (11)$$

For wide range input:

$$V_{IN(PEAK)} = 264V \times \sqrt{2} = 374V \quad (12)$$

The linear range of I_{AC} is 0~360μA. A 1.2M resistor is suggested for a wide input range ($90V_{AC}$ ~ $264V_{AC}$).

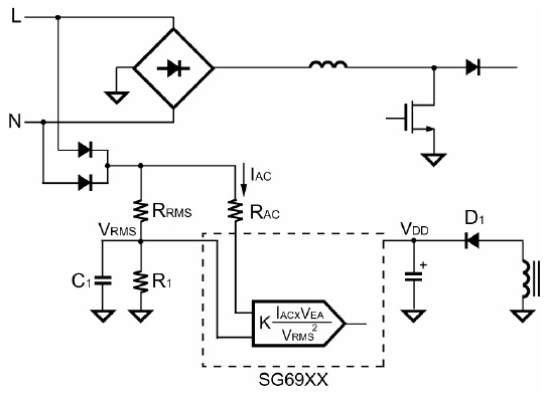

Figure 6. Linear Range

Line Voltage Detection (V_{RMS})

Figure 6 shows a resistive divider with low-pass filter connected to the VRMS pin for line-voltage detection. The V_{RMS} input is used for the PFC multiplier and brownout protection.

For a sine wave input voltage, the voltage on the VRMS pin is directly proportional to input voltage. To achieve the brownout protection, the PFC stage is disabled after a 195ms delay once the V_{RMS} voltage drops below 0.8V. The PWM stage is protected through the open-loop detection on the FBPWM pin when the output voltage of the PFC stage is too low. After that, SG6902 turns off. When V_{RMS} voltage is higher than 0.98V, the SG6902 restarts in accordance with power-on sequence of PFC and PWM stages.

For example, a brownout protection is set as $75V_{AC}$. The R_{RMS} and R_I can be determined as:

$$V_{IN(MEAN)} = V_{IN} \times \sqrt{2} \times \frac{2}{\pi} \quad (13)$$

$$V_{RMS} = \frac{R1}{R1 + R_{RMS}} \times V_{IN} \times \sqrt{2} \times \frac{2}{\pi} \quad (14)$$

The threshold of V_{RMS} = 0.8V. If R_{RMS} = 4.8MΩ and V_{IN} = $75V_{AC}$, the value of R1 is 56.8KΩ.

PFC Operation

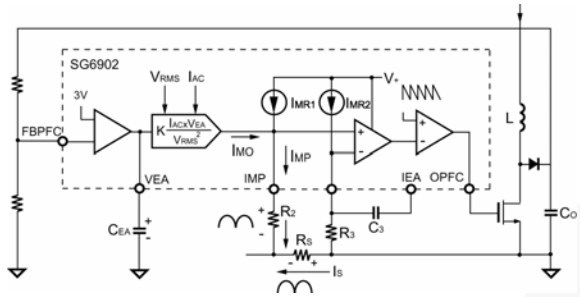

Figure 7. Current Output

The current source output from the switching charge multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad (15)$$

According to Figure 7, the current output from IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. The resistor R_2 is equipped as same as R_3. The constant current source I_{MR1} is identical with I_{MR2}. They are used to bias (pull HIGH) the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground.

Through the differential amplification of the signal across R_S, a better noise immunity is acjoeved. The output of I_{EA} compared with an internal sawtooth generates a switching signal for PFC. Through the feedback loop of the average current control mode, the input current I_S is proportional to I_{MO}:

$$I_{MO} \times R_2 = I_S \times R_S \quad (16)$$

According to this equation, the minimum value of R_2 and maximum value of R_S can be determined. The I_{MO} should be estimated under its specified maximum value.

A concern in determining the value of the sense resistor R_S includes low-resistance R_S reduces the power consumption, but high-resistance R_S provides high resolution to achieve low input current THD (total harmonic distortion). Using a current transformer (CT) instead of R_S improves the efficiency for high-power converters.For a 120W adapter, the power consumption of $R_S = 0.36\Omega$ is:

$$P_{RS} = \left(\frac{120W / 0.85}{90}\right)^2 \times 0.36 = 0.885W \quad (17)$$

R_2 and R_3 can be determined as (the brownout threshold is 75V):

$$I_{MAX} = \frac{120W/0.8}{75V} \times \sqrt{2} = 2.83A$$
$$I_{MO} = \frac{R_S \times I_{MAX}}{R_2} \quad (18)$$
$$I_{MO} = \frac{0.36 \times 2.83}{3.3K} = 308\mu 0$$

The results show that R_S, R_2, and R_3 values are fit for providing 120W output.

Cycle-by-cycle Current Limiting

SG6902 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 8 shows the peak current limit for the PFC stage. The switching signal of PFC stage is turned off immediately once the voltage on ISENSE pin goes below the threshold voltage V_{PK}.

The voltage of V_{RMS} determines the threshold voltage V_{PK}. The correlation of the threshold voltage V_{PK} and VRMS is shown in Figure 8. The amplitude of the constant current I_P shown in Figure 8 is determined by a reference current I_T, in accordance with the following equation as:

$$I_p = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad (19)$$

Therefore, the peak current of the I_S can be expressed as:

$$I_{S\_PEAK} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad (20)$$

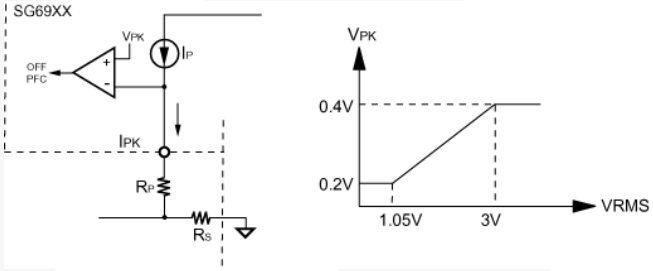

Figure 8. Current Limit

Multi-vector Error Amplifier

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC-value according to Equation 14. In other words, a low-pass RC filtering for V_{RMS} and a narrow bandwidth (lower than the line frequency) of PFC voltage loop are suggested to achieve better input current shaping. The trans-conductance error amplifier has output impedance R_O (>90kΩ). A capacitor C_{EA} (1μF ~ 10μF) is suggested to connect from the output of the error amplifier to ground (Figure 9). A dominant pole f_1 of the PFC voltage loop is shown as:

$$f_1 = \frac{1}{2\pi \times R_O \times C_{EA}} \quad (21)$$

The average total input power can be expressed as:

$$P_{IN} = V_{IN(RMS)} \times I_{IN(RMS)}$$
$$\propto V_{RMS} \times I_{MO}$$
$$\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \quad (22)$$
$$\propto V_{RMS} \times \frac{\frac{V_{IN}}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \propto V_{EA}$$

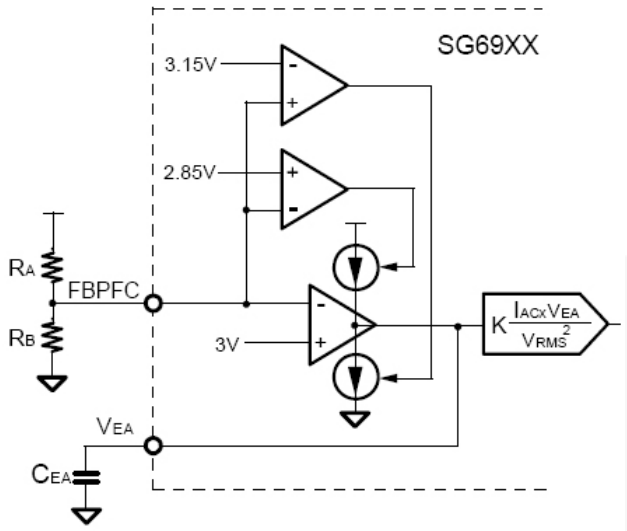

Figure 9. Multi-vector Error Amplifier

Equation 22 shows the output of the voltage error amplifier, V_{EA}, controls the total input power and the power delivered to the load.

Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of PFC output voltage.

Figure 10 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage (FBPFC) exceeds ±5% of the reference voltage (3V), the trans-conductance error amplifier programs its output current to speed up the loop response. If R_A is open circuit, SG6902 is turned off immediately to prevent over-voltage on the output capacitor.

Two-level PFC Output voltage

For universal input ($90V_{AC}$ ~ $264V_{AC}$), the output voltage of PFC is usually designed to 250V at low line and 400V at high line. This improves efficiency of the power converter for low-line input. The RANGE pin (open-drain) is used for the two-level output voltage setting.

Figure 10 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground when the V_{RMS} voltage exceeds 1.95V. It is a high-impedance output (open) whenever the V_{RMS} voltage drops below 1.6V. The output voltages can be determined using below equations:

$$\text{Range} = \text{Open} \Rightarrow V_O = \frac{R_A + R_B}{R_B} \times 3V \quad (23)$$

$$\text{Range} = \text{GND} \Rightarrow V_O = \frac{R_A + (R_B // R_C)}{(R_B // R_C)} \times 3V \quad (24)$$

Determine the resistor divider ratio R_A/R_B:

$$\frac{R_A}{R_B} = \frac{V_O}{3} - 1 \quad (25)$$

$$\frac{R_A}{R_B} = \frac{250}{3} - 1 = 82.33 \quad (26)$$

Assume R_A = 3MΩ, R_B = 36.5KΩ, and R_C = 60KΩ. *Refer to Figure 10*. At high line input, maximum output voltage is:

$$V_{O(MAX)} = 3.15\times = \left(\frac{R_A}{R_B // R_C} + 1\right) = 420V \quad (27)$$

Another circuit provides further over-voltage protection to inhibit the PFC switching once the feedback voltage exceeds the 3.25V the output voltage is clamped at:

$$V_{O(OVP)} = 3.25 \times \left(\frac{R_A}{R_B // R_C} + 1\right) = 433V \quad (28)$$

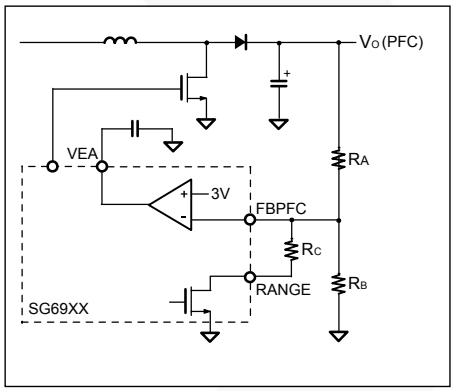

Figure 10. Feedback Voltage of PFC

PWM SECTION

Soft-starting the PWM stage

The soft-start pin controls the rising time of the output voltage and prevents the overshoot during power on. The soft-start capacitor value for the soft-start period t_{SS} is given by:

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{OZ}} \quad (29)$$

where V_{OZ} is the zero-duty threshold of FBPWM voltage.

Leading-Edge Blanking (LEB)

A voltage signal develops on the current-sense resistor R_S represents the switching current of MOSFET. Each time the MOSFET turns on, a spike, caused by the diode reverse recovery time and by the parasitic capacitances of the MOSFET, appears on the sensed signal. The SG6902 has a build-in leading-edge blanking time of about 350ns to avoid premature termination of MOSFET by the spike. Only a small-value RC filter (e.g. 100Ω + 47pF) is required between the IPWM pin and R_S to prevent negative spike into the IPWM pin. A non-inductive resistor for the R_S is recommended.

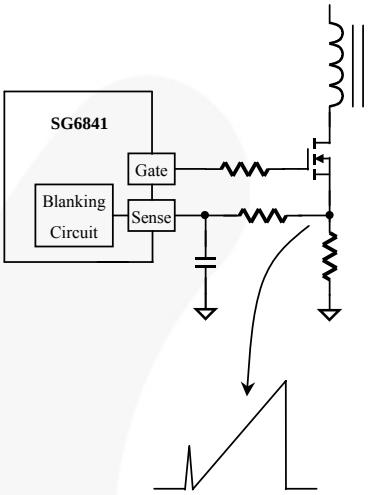

Figure 11. Turn-on Spike

Flyback PWM and Slope Compensation

As shown in Figure 12, peak-current-mode control is utilized for flyback PWM. The SG6902 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation reduces the current loop gain and ensures stable operation for current-mode operation.

When the IPWM voltage, across the sense resistor, reaches the threshold voltage, 0.65V or 0.7V selected by RANGE, the OPWM turns off after a small propagation delay, t_{PD-PWM}. This propagation delay introduces an additional current proportional to $T_{PD-PWM} \bullet V_{PFC}/Lp$, where V_{PFC} is the output voltage of PFC and Lp is the magnetized inductance of flyback transformer. Since the propagation delay is nearly constant, higher V_{PFC} results in a larger additional current and the output power limit is higher than that of the low V_{PFC}. To compensate for this variation, the peak current threshold is modulated by the RANGE output. When RANGE is shorted to GND, the PFC output voltage is higher and the corresponding threshold is 0.65V. When RANGE is opened, the PFC output voltage is lower and the corresponding threshold is 0.7V. Increasing the inductance of transformer improves this phenomenon.

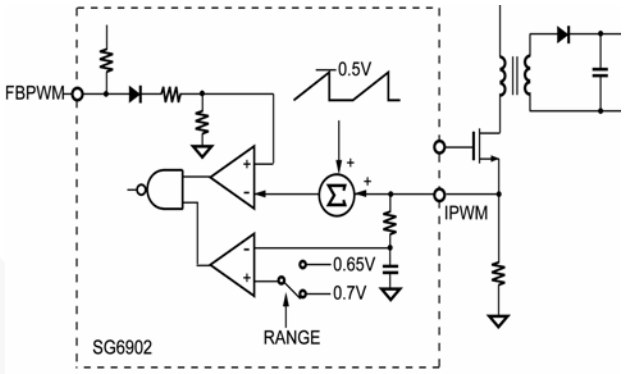

Figure 12. Current Limit and Slope Compensation

Output Driver of OPFC and OPWM

SG6902's OPFC and OPWM is fast totem-pole gate driver that is able to directly drive external MOSFET. An internal Zener diode clamps the driver voltage under 18V to protect MOSFET from over-voltage damage.

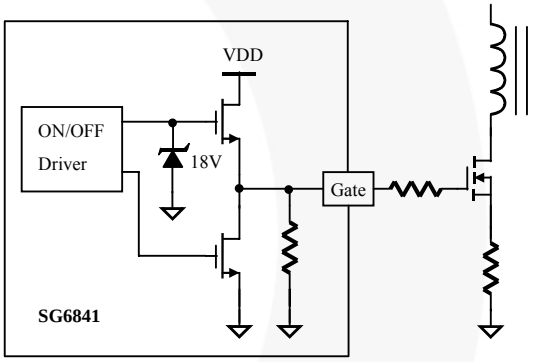

Figure 13. Gate Drive

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

OCP and SCP are based on detection of feedback signal on FBPWM pin. Shown in Figure 14, if over-current or short-circuit occurs, FBPWM is pulled HIGH through the feedback loop. If the FB voltage is higher than 4.5V for longer than 56ms debounce time, SG6902 is turned off. Once V_{DD} is lower than the turn-off threshold voltage, such as 10V, SG6902 is UVLO (under-voltage lockout) shut down. By the startup resistor, V_{DD} is charged (up to the turn-on threshold voltage 16V) until SG6902 is enabled again. If the overloading condition still exists, the protection takes place repeatedly. This prevents the power supply from being overheated in overloading condition. The 650ms time-out signal prevents SG6902 from being latched off when the input voltage is fast on/off.

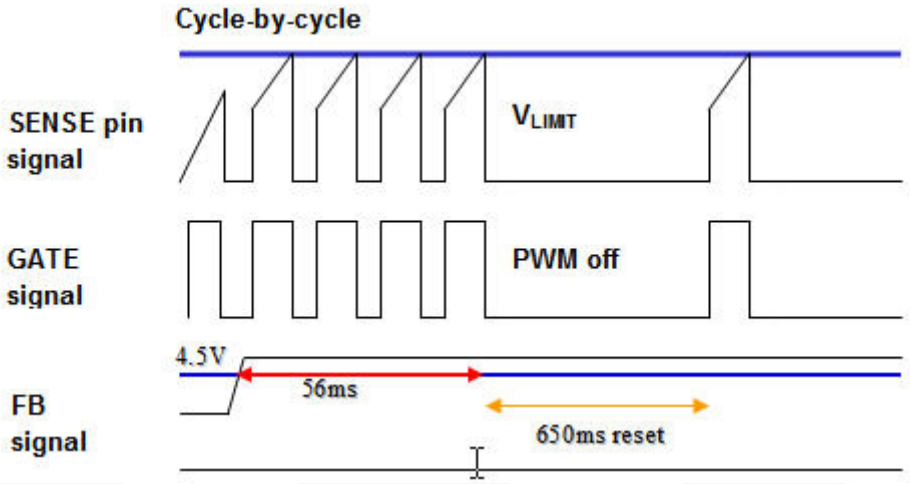

Figure 14. Over-Current Protection or Short-Circuit Protection

Over-Temperature Protection (OTP)

SG6902 provides an OTP pin for over-temperature protection. A constant current is output from this pin. If RI is equal to 24kΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to ground as shown in Figure 15. When the OTP voltage drops below 1.2V, SG6902 is disabled until OTP voltage exceeds 1.4V.

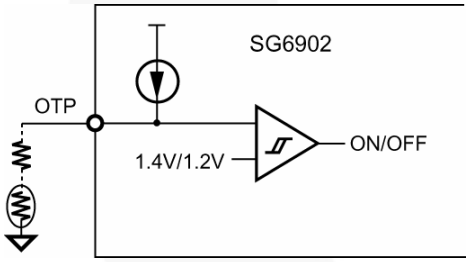

Figure 15. Over-Temperature Protection

Flyback Transformer Design

The turn ratio n = Np/Ns, is an important parameter for a flyback power converter. It affects the maximum duty of the switching signal when the input voltage is in minimum value. It also influences the voltage stresses of the MOSFET and the secondary rectifier.

Refer to Equations 30 and 31. If n increases, the voltage stress of the MOSFET increases; however, the voltage stress of the secondary rectifier decreases accordingly.

$$V_{DS.max} = V_{IN.max} + n \times (V_O + V_f) \quad (30)$$

$$V_{AK.max} = \frac{V_{IN.max}}{n} + V_O \quad (31)$$

where V_f is the forward voltage of output diode and $V_{IN.max}$ = 400V.

Referring to the maximum duty cycle and minimum input voltage at full load, the transformer inductance can be calculated as:

$$D_{max} = \frac{n \times (V_O + V_f)}{V_{IN.min} + n \times (V_O + V_f)} \quad (32)$$

$$L_P = \frac{\eta \times (V_{IN max} \times D_{max})^2}{2 \times P_{OUT} \times f_S \times B_r} \quad (33)$$

where B_r is how much percentage of the output power is into CCM in low line input voltage. Normally, the B_r is set as 30% ~ 50%. $V_{IN.min}$ = 250V.

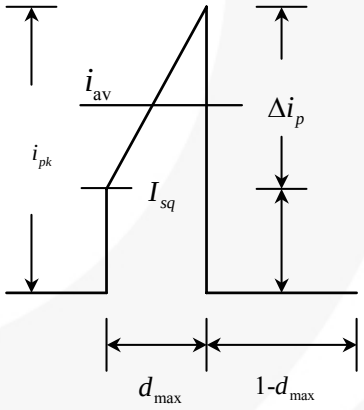

Figure 16. Primary Current Waveform

Figure 16 shows the primary current waveform. Once the inductor L_P is determined, the primary peak current I_{pk} and average current I_{av}, at the full load and low line input voltage, can be expressed as:

$$I_{AV} = \frac{P_O}{\eta \times V_{IN.max} \times D_{max}} \quad (34)$$

$$\Delta I_P = \frac{V_{IN.max}}{L_P} \times D_{max} \times T_S \quad (35)$$

$$I_{PK} = \frac{\Delta I_P}{2} + I_{AV} \quad (36)$$

$$I_{SQ} = I_{PK} - \Delta I_P \quad (37)$$

From Faraday's law, the turns of primary side can be expressed as:

$$N_P = \frac{L_P \times I_{PK}}{B_{max} \times A_e} \times 10^8 \quad (38)$$

The turns of auxiliary winding can be expressed as:

$$N_{aux} = \frac{N_P \times (V_{DD} + V_{fa}) \times (1 - D_{max})}{V_{IN.max} \times D_{max}} \quad (39)$$

where V_{DD} is set to around 12V and V_{fa} is the forward voltage of V_{DD} rectifier diode.

Transformer Winding Structure

The auxiliary winding of the transformer is developed to provide a power source (V_{DD} voltage) to the control circuit. To produce a regulated V_{DD} voltage, the reflected voltage of the auxiliary winding is designed to correlate to the output voltage of secondary winding. A switching voltage spike, caused by the leakage inductance of the primary winding, would be coupled to the auxiliary winding to increase the V_{DD} voltage in response to the increase of the load.

When the V_{DD} voltage is increased higher than the voltage of the over-voltage protection 24.5V, the control circuit turns off the PWM and PFC stages to protect the power supply. Therefore, the transformer windings should prevent the auxiliary winding from primary winding interference.

Figure 17 shows a transformer winding structure, including primary winding (Np1), copper layer (shield), secondary winding (Ns), auxiliary winding (AUX), copper layer (shield), and primary winding (Np2). Because the auxiliary winding is between secondary winding and shield windings, it can alleviate the variation of V_{DD} voltage and avoid the V_{DD} voltage reaching the over-voltage threshold of 24.5V for normal operation.

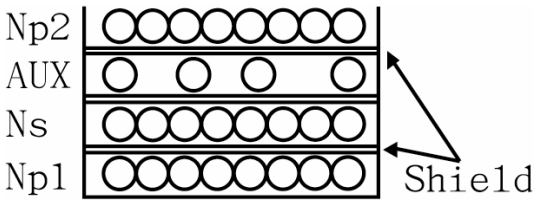

Figure 17. Winding Structure

Lab Note

Before rework or solder/desolder on the power supply, discharge primary capacitors by external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during solder/desolder.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1

Printed Circuit Board Layout

Note that SG6902 has two ground pins. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6902. A resistor (5 ~ 20Ω) is recommended, connected in series from the OPFC and OPWM to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 18 shows an example of the PCB layout. The *ground trace* connected from the AGND pin of SG6902 to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 1* provides a signal ground. It should be connected directly to the decoupling capacitor V_{DD} and/or to the AGND pin of the SG6902. The *ground trace* 2 shows that the AGND pins should connect to the PFC output capacitor C_O independently. The *ground trace 3* is independently tied from the PGND to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching.

To provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The IPFC pin is connected directly to R_S through R_3 to improve noise immunity (beware that it may incorrectly be connected to the ground trace 2). The IMP and ISENSE pins should also be connected directly via the resistors R_2 and R_P to another terminal of R_S. Due to the *ground trace 4 and 5* is PFC and PWM stages Current loop, which should be as short as possible.

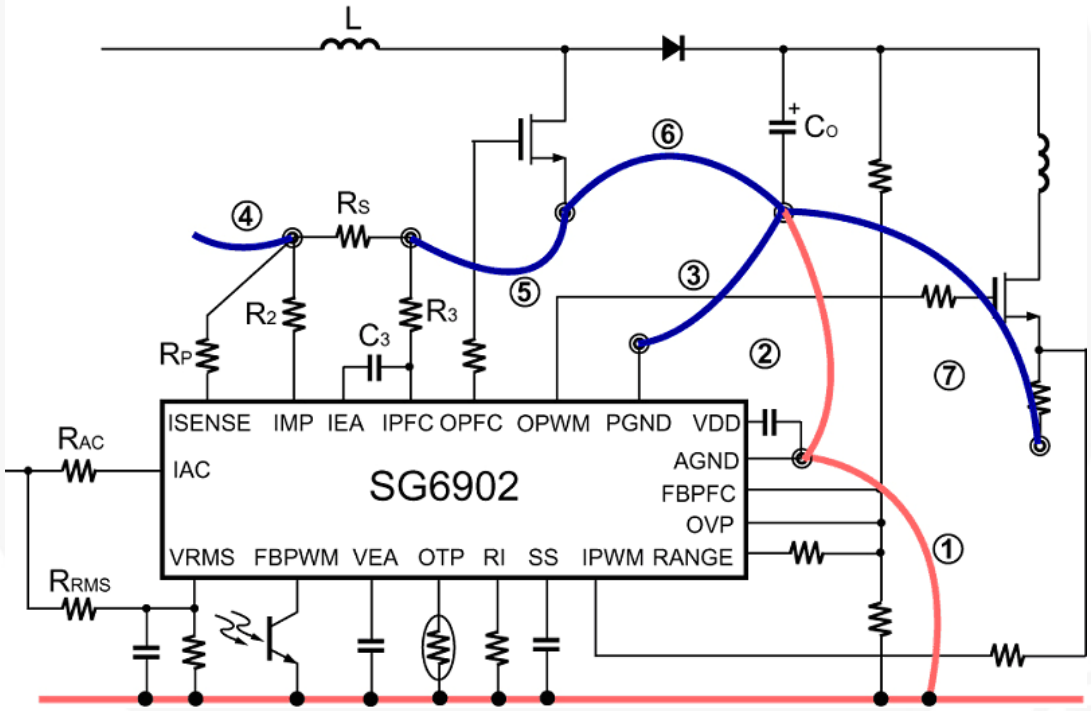

Figure 18. PCB Layout

Related Datasheets

SG6902 — Green Mode PFC / Flyback PWM Controller
SG6901A — Green Mode PFC / Flyback PWM Controller